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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY. DOCKET NO.	CONFIRMATION NO.
09/867,064	05/29/2001	Matthew J. Adiletta	10559-468001 / P10673	6308

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FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
RIZZUTO, KEVIN P	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/867,064	ADILETTA ET AL.	
	Examiner	Art Unit	
	Kevin P Rizzuto	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *5/29/01, 7/16/0, and 12/16/021*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10, 12-15* is/are rejected.

7)☒ Claim(s) *12-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-10 and 12-15 have been examined.

2. Acknowledgement of papers filed: application on 5/29/01, Oath/Declaration on 7/16/01 and Change of Address on 12/16/02. The papers filed have been placed on record.

Priority

3. It is acknowledged that application is a continuation of application no. 09/473,799, filed on December 28, 1999, and claims priority under 35 U.S.C. 120.

Specification

4. The disclosure is objected to because of the following informalities: Grammar error on line 5 of page 16. Line 15 should state "supported" instead of "support".

Appropriate correction is required.

5. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: "Method and apparatus for low overhead multithreaded communication in a parallel processing environment including inter-thread messages for thread data addresses and using a register that is cleared upon reading to indicate message and thread status."

Claim Objections

6. As per claims 12-15, the numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not). There is no claim 11 therefore the numbering of claims is not consecutive and claims 12-15 are objected to.

7. Claim 14 is objected to for improper grammar. "Further comprises instruction causing" is not proper grammar.

8. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claim 12 recites the limitation "the processor of claim 11" in line 1. There is insufficient antecedent basis for this limitation in the claim and other limitations because there is no claim 11. Examiner is unable to interpret and examine claim 12 because it is unknown if it was intended to be dependent on a different claim or if claim 11 is in fact missing. Claim 12 will be treated as dependent on claim 7.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1-7, 9, 10 and 13-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Sites, U.S. Patent 5,193,167.

13. As per claim 1, a method of inter-thread communication in a multi-threaded computer (The CPUs share a memory and system bus and each can execute sequential instructions, therefore the system of Sites is multi-threaded, figure 1) comprises:

-Storing an inter-thread message in memory (address in physical address register 95), the inter-thread message having a field for an address that indicates a location of data for a next thread to execute: (CPU 10 (current thread) stores the address of data that CPU 15 (next thread) is to execute when CPU 10 executes a LDQ_L instruction (column 15, lines 6-30). Then, after CPU 15 executes a LDQ_L instruction, it will monitor CPU 10's physical address register 95 to check if there is a match, when there is a match, the address stored in physical address register 95 is also the address of data that is for CPU 15.

-And writing to a self-destruct register (lock flag 96) after storing the message (address in physical address register 95), to indicate that a thread which stored the message in memory has completed execution, with the self-destruct register being cleared upon reading by the next thread: (Thread is defined as, "A single sequential flow of control within a process." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) The lock flag 96 is written to when the current thread executes LDQ_L, the current thread is defined as the instructions leading up to and including LDQ_L, since that is a sequential flow of control within a process. Therefore, since the lock flag 96 is set when LDQ_L is completed, and LDQ_L is the end of the current thread, it indicates that the thread has completed execution. When the next thread executes a STQ_L instruction, the lock flag 96 is read and cleared. (Column 15, lines 5-30))

14. As per claim 2, the method of claim 1 wherein the inter-thread message field for an address provides an address of a register where the data for the next executing thread is stored (Column 15, lines 5-30; The address in physical address register 95 contains the address where the data in an operand of the next executing thread is stored. The address is for a memory location of a specified size that contains data, which by the definition in the IEEE dictionary, is a register. A register is "a storage device or storage location having a specified storage capacity." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.)

15. As per claims 3 and 9, the method of claim 1 wherein writing to a self-destruct register further comprises: setting at least one bit in the self-destruct

register which corresponds to the thread which is writing to the self-destruct register. (Column 15, lines 5-30 and figure 5; The lock flag 96 is a register that has a bit set that corresponds to the thread that is writing to it.)

16. As per claims 4 and 10, the method of claim 1 wherein writing to a self-destruct register further comprises: setting one bit in the self-destruct register which corresponds to the thread which is writing to the self-destruct register. (Column 15, lines 5-30 and figure 5; The lock flag 96 is a register that has a bit set that corresponds to the thread that is writing to it.)

17. As per claim 5, the method of claim 1 further comprising:

-Writing to the self-destruct register by a first thread (Column 15, lines 5-30; the instruction stream in CPU 10 that includes instructions leading up to and including LDQ_L is a first thread. The LDQ_L instruction writes to the lock flag 96.)

-Reading from the self-destruct register by a second thread: (Column 15, lines 5-30; the instruction stream in the CPU 15 including the STQ_L instruction is the second thread. The second thread's STQ_L instruction will read the lock flag 96)

-Where the reading further comprises: reading bits, if any, that are set in the self-destruct register; and clearing all of the bits of the self-destruct register (Column 15, lines 5-30; The lock flag 96 is read by the second thread and it is cleared afterwards)

18. As per claim 6, the method of claim 5 further comprises:

-Reading the inter-thread message from the memory by a new thread (The inter-thread message is the address stored in physical address register 95. The inter-thread message is inherently read by the new thread (the second thread) in order to monitor physical address register 95 and detect a match of addresses.)

-Where the new thread is a thread other than the first thread; and executing the new thread. (The CPUs monitor other CPUs' physical address registers 95 to detect a match. The new thread, on CPU15, checks the other threads (other CPU's) when it is executing.)

19. As per claim 7, a hardware-based multi-threaded processor comprises:

-A general purpose processor that coordinates system functions (figure 1, CPU 10, it is inherent that CPU 10 coordinates system functions within CPU 10. For example, controlling the processing of instructions, including fetching, decoding, issuing and executing, is the coordinating system functions).

-A plurality of microengines that support multiple thread execution (Figure 1, CPU 15 and the CPU adjacent CPU 15; When each has an instruction stream, multiple thread execution is present.)

-A scratchpad memory for storing inter-thread messages (physical address register 95) where execution of a write to the scratchpad memory by a first thread causes an address to be stored as an inter-thread message which

indicates a location of data for a new thread: (CPU 10 (executes first thread) stores the address of data that CPU 15 (executes a new thread) is to execute when CPU 10 executes a LDQ_L instruction (column 15, lines 6-30) and CPU 15 executes a LDQ_L instruction after, then CPU15 will monitor CPU 10's physical address register 95 to check if there is a match, when there is a match, the address stored in physical address register 95 is also the address of data that is for CPU 15. Scratchpad memory is a temporary memory storage device, and therefore physical address register 95 is a scratchpad memory.)

-And a self-destruct register for indicating the execution status of threads where reading of the self-destruct register clears all of the bits of the self-destruct register: (Thread is defined as, "A single sequential flow of control within a process." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) The lock flag 96 is written to when the first thread executes LDQ_L, the first thread is defined as the instructions leading up to and including LDQ_L. Therefore, since the lock flag 96 is set when LDQ_L is completed, and LDQ_L is the end of the first thread, it indicates that the thread has completed execution, which is the status of an executing thread. When the next thread executes a STQ_L instruction, the one and only bit of lock flag 96 is read and cleared. (Column 15, lines 5-30))

20. As per claim 12, the processor of claim 7, wherein the read from the self-destruct register by the thread causes execution of a new thread for each bit that is set, if any, in the self-destruct register: (The lock flag is only one bit, it can be

set or cleared. Thread is defined as, "A single sequential flow of control within a process." (The Authoritative Dictionary of IEEE Standard Terms, 7th ed.) The lock flag 96 is written to when the current thread executes LDQ_L, the current thread is defined as the instructions leading up to and including LDQ_L on CPU10, since that is a sequential flow of control within a process. A new thread (defined as the store operation of the STQ_L instruction and the instructions following it on CPU10) is executed if the lock flag register of the CPU that the STO_L is being processed in is set. If it is not set, the STO_L instruction does not complete the store, and therefore the new thread does not execute because the store does not take place.)

21. As per claim 13, a computer program product residing on a computer readable medium causing a processor to perform a function comprises instructions causing the processor to: store an inter-thread message in memory (Address stored in physical register 95); and set at least one bit in a self-destruct register (Lock Flag register 96): (It is inherent that the processor of Sites must be operated by code that makes up a computer program product residing on a computer readable medium. Each CPU runs its own instructions and the instructions make up a thread. Different CPUs monitor and inherently read other CPUs' physical registers 95 in order to detect a match. Since CPUs are reading other CPUs' physical registers 95, the data in the physical register 95 is an inter-thread message in memory.) (Column 14, line 64 to column 15, line 53)

22. As per claim 14, the computer program of claim 13 further comprises instructions causing the processor to: store a register address as the inter-thread message in memory. (The inter-thread message is stored in physical register 95, which is a memory device. The message stored is an address that points to a location in memory. A location in memory is "capable of retaining information, often that contained in a small subset (for example, on word), of the aggregate information in a digital computer", which is the definition of a register (The Authoritative Dictionary of IEEE Standards Terms, 7th ed.).

23. As per claim 15, the computer program of claim 13 further comprises instructions causing the processor to: read the contents of the self-destruct register, the read also clearing the self-destruct register; and execute a new thread according to any bits set in the self-destruct register. (The lock flag 96 is written to when the first thread executes LDQ_L, the first thread is defined as the instructions leading up to and including LDQ_L executing on CPU 10. Therefore, since the lock flag 96 is set when LDQ_L is completed, and LDQ_L is the end of the first thread, it indicates that the thread has completed execution, which is the status of an executing thread. When the next thread (instructions executed on CPU 15) executes a STQ_L instruction, the one and only bit of lock flag 96 is read and cleared. However, if a new thread is executing and the lock flag 96 is not set, it does not clear the lock flag. Therefore, the new thread is executed according to the bits set.) (Column 15, lines 5-30))

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claim 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Sites, U.S. Patent 5,193,167 in view of Panwar, U.S. Patent 5,870,597.

26. As per claim 8, Sites teaches the processor of claim 7 wherein the plurality of microengines further comprise: executing a write to the scratchpad memory (Physical address register 95) by the first thread to cause an address of data for a next thread to be stored.

27. However, Sites fails to teach that a first thread causes an inter-thread message that includes an address indicating the location of the register stack.

28. Panwar teaches an inter-thread message stored in Current Window Pointer (CWP) register 306 (also labeled as CWP 610 in figure 6). It is an inter-thread because multiple processes (threads) read and write to it. The address stored in the CWP register points to a window of registers (a register stack). Upon a Restore command, the CWP register is written to by the current process to indicate an address of a different process' window of registers. The CWP register is the scratchpad memory because it temporarily holds addresses and then is updated to new addresses. The process that executes the Restore

command (write) is the first thread. The register window that the restored CWP register points to is for the new thread. (Column 7, line 40 to Column 8, line 5)

29. One of ordinary skill in the art at the time of the invention would have recognized that having a register window for each process allows fewer bits to be needed to address logical registers in a process. If all registers were addressable in the whole register file instead of only those within each process' window, more bits would be needed to specify an individual register. Therefore, a benefit of Panwar's register windowing is fewer bits are needed to encode instructions in order to address them in a process. For example, Panwar uses 32-register windows, and in turn, five bits are needed to address a register in a window. Without a window, and 128 registers available as shown in figure 3, it would take 7 bits to address a specific register. (Background of the invention, columns 2 and 3). Also, one of ordinary skill in the art at the time of the invention would have recognized having one shared register file reduces the total number of registers needed, for instance, 5 processes each with 32 registers would need 160 registers, while Panwar implements a smaller, shared 128-register register file. Sites implements multiple register files for each CPU, 64 registers for each CPU, 32 for the execution unit and 32 for the floating-point unit (column 7, lines 20-28 and column 8, lines 55-61). With multiple CPUs, the amount of registers increases and becomes more costly in terms of money and chip space. One of ordinary skill in the art at the time of the invention would have recognized a shared register file would reduce the cost and size of the register file in the computer system and windowing in the shared register file would reduce the size

of addresses for the register file to the amount needed to access only those in the window, thus preventing the increase in the instruction and program size.

30. It would have been obvious to combine the shared register file with register windows of Panwar and the computer system of Sites in order to reduce the cost and size of the register file hardware. This benefit would have provided motivation to one of ordinary skill in the art to combine the inventions.

Conclusion

31. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin P Rizzuto whose telephone number is (571)272-4174. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571)272-4174. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KPR

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100